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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/573,689 | 03/27/2006 | Makoto Sasaki | L9289.06125 | 7145 |

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| EXAMINER | |
|---|---|
| JOHNSON, RYAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2817 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/573,689 | SASAKI, MAKOTO | |
| | Examiner | Art Unit | |
| | Ryan J. Johnson | 2817 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 March 2006 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 3/27/06.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

2. No copies of JP2002050979 or JP04249920 listed on the IDS filed 3/27/2006 were received. However, the examiner was able to obtain abstracts of both references and both references were considered.

### *Specification*

3. The abstract of the disclosure is objected to because it is longer than 15 lines and 150 words. Correction is required. See MPEP § 608.01(b).

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1,2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vilhonen et al. (U.S. Patent No. 6,972,633, hereinafter Vilhonen) in view of Chengson (U.S. Patent No. 6,538,518).

6. Claim 1: Vilhonen discloses a PLL frequency synthesizer (Fig.1) comprising:

a loop filter with different cutoff frequencies (loop filter 23 has different cutoff frequencies depending on the tuned capacitance of C2 and C3);

an oscillation section (24) that generates a frequency signal corresponding to a voltage output from the loop filter (col.3,36-47);

a variable frequency fluctuation component elimination circuit (4) that is provided between said oscillation section and an oscillation signal output terminal (since the filter is a base-band filter of the transmitter chain; col.2,65-67), it must inherently be located between the VCO of the PLL, 24, and the oscillation signal output terminal, the output of the baseband filter) and that eliminates a frequency fluctuation component that varies for the loop filter (a filter inherently eliminates a frequency fluctuation component based on its cutoff frequency determined by the variable capacitance within the filter. This frequency fluctuation varies depending on the frequency of the signal and the cutoff frequency of both filters).

a control section (3) that performs control of said frequency fluctuation component elimination circuit in accordance with changing of the loop filter (the calibrating system changes both the loop filter capacitance values as well as the base-band filter capacitance values in accordance with a common temperature condition; col.3,56-col.4,20).

Vilhonen discloses the variable capacitors in the loop filter. Vilhonen does not explicitly disclose that the loop filter contains a plurality of switched looped filters. Chengson discloses selecting from a plurality of loop filters (202,203). Choosing a multiple switched loop filter system over a single variable loop filter system is a mere design choice, as either system performs the identical function of adjusting the filter time constant. Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to have used multiple switching loop filters as disclosed by Chengson in the system of Vilhonen in order to have provided an obvious design choice alternative to the system of Vilhonen.

7. Claim 2: Vilhonen discloses that the frequency fluctuation component elimination circuit comprises a variable capacitance capacitor (C4) whereby self-resonance is performed with different frequency fluctuation components (the cutoff frequency changes depending on the calibrating component 3, thus the filter performs its function on different frequency components depending on the calibration value).

8. Claim 5: Vilhonen discloses that the PLL is used in a radio apparatus (col.2,59-64).

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vilhonen et al. (U.S. Patent No. 6,972,633, hereinafter Vilhonen) in view of Chengson (U.S. Patent No. 6,538,518) as applied to claim 1 above, and further in view of Csicsatka (U.S. Patent No. 3,934,092). Vilhonen and Chengson disclose the limitations of claim 1. Vilhonen also discloses that the filtering is performed on different frequency fluctuation components (depending on the changes in capacitance by the calibration component). Vilhonen and Chengson do not explicitly disclose that the frequency fluctuation component elimination circuit comprises a resonance circuit. Csicsatka discloses using a resonance circuit that acts as a band-pass filter (Fig.10) in a transceiver device. It is well known in the art that using inductors and capacitors a band-pass filter provides a filter with a higher Q factor. Therefore, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to have used the band-pass filter as disclosed by Csicsatka as the baseband filter in the circuit of Vilhonen in order to have provided a well-known band-pass filter with a higher Q factor.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vilhonen et al. (U.S. Patent No. 6,972,633, hereinafter Vilhonen) in view of Chengson (U.S. Patent No. 6,538,518) as applied to claim 1 above, and further in view of Ohira (U.S. Patent No. 6,252,468). Vilhonen and Chengson disclose the limitations of claim 1, but do not explicitly disclose resistors provided between the oscillation section and the junction point, on the feedback signal line, or on the output line. Ohira discloses using three resistors output from a VCO in a PLL in a similar attenuating circuit (6 of Figure 2) in order prevent mixers in a receiver from being affected by the output impedance of the VCO (col.1,53-67). Although Ohira lacks a resistor on the feedback signal line, the overall functionality of the circuit remains the same and using a resistor on the feedback line rather than a resistor connected to ground, as disclosed by Ohira, is a mere manner of design choice. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used three resistors as an attenuating circuit, as disclosed by Ohira, in the transceiver of Vilhonen in order to have prevented mixers in a transceiver being affect by the output impedance of the VCO.

***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lu (U.S. Patent No. 6,538,499) and Nakatani et al. (U.S. Patent No. 6,441,692) disclose output band-pass filters in a PLL.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J. Johnson whose telephone number is 571-270-1264. The examiner can normally be reached on Monday - Thursday, 9:00 am - 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RJJ/

Robert Pascal
Supervisory Patent Examiner
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